# USB to Dual Serial Ports Chip CH9103

Datasheet

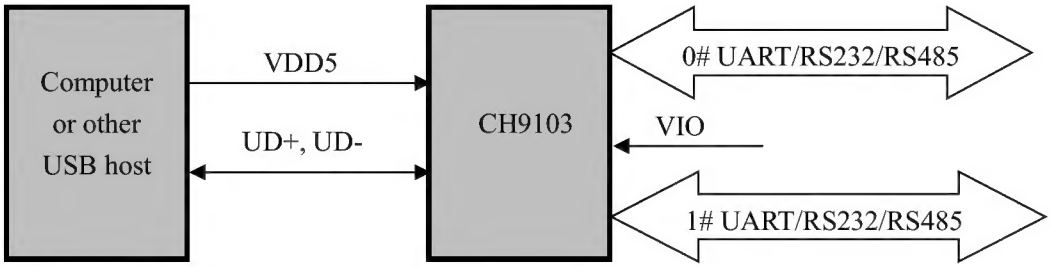
Version: 1A

http://wch.cn

## 1. Overview

CH9103 is a USB bus converter chip which converts USB to dual asynchronous serial ports.

Each serial port supports high-speed full-duplex, supports parity check, provides partial MODEM signals, used to extend serial ports for computers, or upgrade directly from normal serial devices to USB bus.

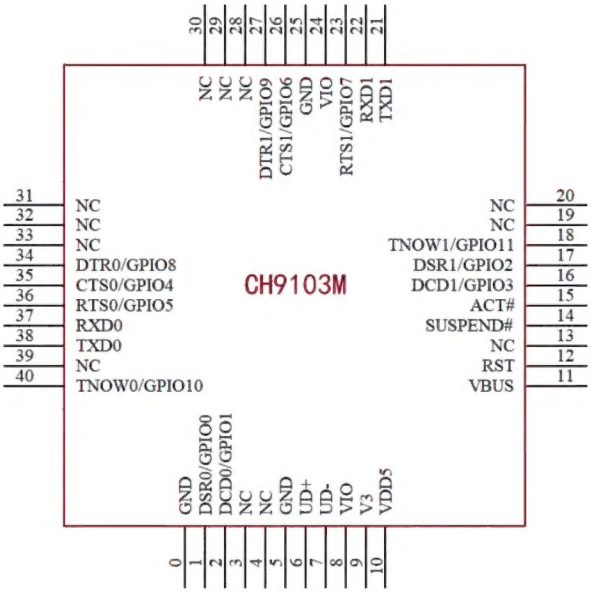



## 2. Features

- Full-speed USB device interface, USB 2.0 compatible.
- Built-in firmware, emulate standard UART interface, used to upgrade the original serial peripheral or expand additional serial port via USB.
- Original UART applications are totally compatible without any modification in Windows operating systems.
- Supports free installation OS which built-in CDC driver or multi-functional high-speed VCP vendor driver.
- Dual hardware full duplex UART interface, integrated independent transmit-receive buffer, supports communication baud rate varies from 50bps to 3Mbps.
- Supports 5, 6, 7, 8 data bits, supports odd, even, space, mark and no parity.
- Supports common MODEM signals RTS, DTR, DCD, DSR and CTS.
- Supports CTS and RTS hardware automatic flow control.
- Supports half-duplex, provides sending status TNOW which supports RS485 switching.
- Supports RS232 interface, through external voltage conversion chip.
- USB side supports 5V and 3.3V power supply voltage.
- Serial port and I/O powered independently, supports 5V, 3.3V, 2.5V and 1.8V power supply voltages.
- Built-in power-on reset, built-in clock, no external crystal required.
- Built-in EEPROM, parameters such as chip VID, PID, maximum current value, vendor and product information string can be configured.
- Built-in Unique ID (USB Serial Number).

- RoHS compliant QFN40 lead-free package.

## 3. Package




| Package | Body size | Lead pitch | | Description | Part No. |
|---|---|---|---|---|---|
| QFN40_6X6 | 6*6mm | 0.5mm | 19.7mil | Square leadless 40-pin patch | CH9103M |

Note:

The EPAD is 0# pin GND, optional but recommended to connect; other GNDs must be connected.

USB transceiver of CH9103 is designed in accordance with the USB2.0 full built-in design, UD+ and UD- pins cannot connect with resistor in series, otherwise, it will affect the signal quality.

## 4. Pin definitions

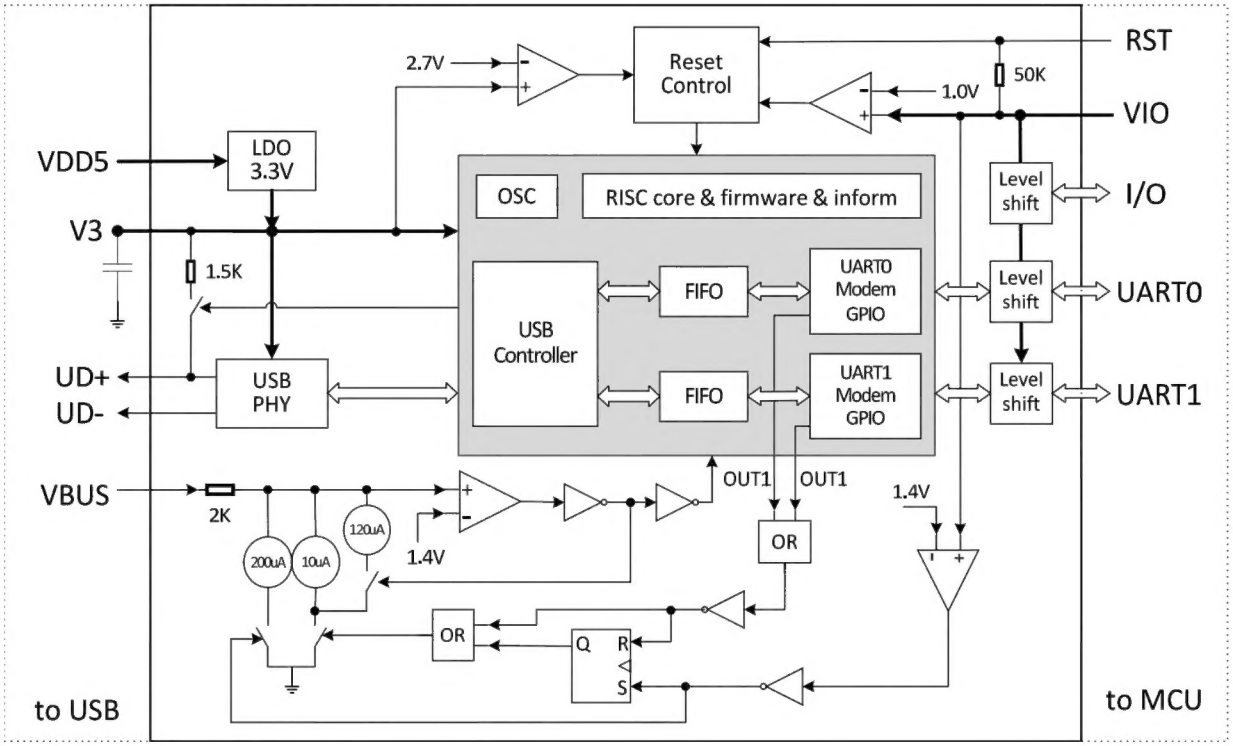
| Pin No. | Pin Name | Pin Type | Pin Description |
|---|---|---|---|
| 10 | VDD5 | POWER | Power supply voltage input, requires an external decoupling capacitor |
| 8, 24 | VIO | POWER | I/O power supply voltage input, requires an external decoupling capacitor |
| 0, 5, 25 | GND | POWER | Ground, connected to ground of USB bus directly |
| 9 | V3 | POWER | Internal power regulator output, core and USB power input, When VDD5 voltage is less than 3.6V, connected to VDD5 to input the external power supply, an external power decoupling capacitor is required to be connected when the VDD5 voltage is greater than 3.6V |
| 12 | RST | IN | Input of external reset, active low, built-in pull-up resistor |

| | | | |
|---|---|---|---|
| 6 | UD+ | USB signal | Connect to USB D+ Signal **directly**, do not connect resistor in series |
| 7 | UD- | USB signal | Connect to USB D- Signal **directly**, do not connect resistor in series |
| 11 | VBUS | IN | VBUS status detection input of USB bus, built-in pull-down resistor |
| 38 | TXD0 | OUT | Transmit asynchronous data output of UART0, high when idle |
| 37 | RXD0 | IN | Receive asynchronous data input of UART0, built-in pull-up resistor |
| 35 | CTS0/<br>GPIO4 | IN /<br>(IN/OUT) | MODEM0 input signal, clear to send, active low<br>General GPIO4, input and output controlled by driver software |
| 34 | DTR0/<br>GPIO8 | OUT /<br>(IN/OUT) | MODEM0 output signal, data terminal ready, active low<br>General GPIO8, input and output controlled by driver software |
| 36 | RTS0/<br>GPIO5 | OUT /<br>(IN/OUT) | MODEM0 output signal, request to send, active low<br>General GPIO5, input and output controlled by driver software<br>**Note:** If RTS0 detects an external pull-down resistor is connected during power-on, disable internal EEPROM configuration parameter, enable chip default parameter |
| 40 | TNOW0/<br>GPIO10 | OUT /<br>(IN/OUT) | UART0 ongoing data transmission status indicator, active high<br>General GPIO10, input and output controlled by driver software<br>**Note:** TNOW function is disabled by default, If TNOW0 detects an external pull-down resistor is connected during power-on, TNOW function will be enabled |
| 1 | DSR0/<br>GPIO0 | IN /<br>(IN/OUT) | MODEM0 input signal, data set ready, active low<br>General GPIO0, input and output controlled by driver software |
| 2 | DCD0/<br>GPIO1 | IN /<br>(IN/OUT) | MODEM0 input signal, data carrier detect, active low<br>General GPIO1, input and output controlled by driver software |
| 21 | TXD1 | OUT | Serial data output of UART1, high when idle |
| 22 | RXD1 | IN | Serial data input of UART1, built-in pull-up resistor |
| 26 | CTS1/<br>GPIO6 | IN /<br>(IN/OUT) | MODEM1 input signal, clear to send, active low<br>General GPIO6, input and output controlled by driver software |
| 27 | DTR1/<br>GPIO9 | OUT /<br>(IN/OUT) | MODEM1 output signal, data terminal ready, active low<br>General GPIO9, input and output controlled by driver software |
| 23 | RTS1/<br>GPIO7 | OUT /<br>(IN/OUT) | MODEM1 output signal, request to send, active low<br>General GPIO7, input and output controlled by driver software |
| 18 | TNOW1/<br>GPIO11 | OUT /<br>(IN/OUT) | UART1 ongoing data transmission status indicator, active high<br>General GPIO11, input and output controlled by driver software |

| | | | |
|---|---|---|---|
| 17 | DSR1/<br>GPIO2 | IN /<br>(IN/OUT) | MODEM1 input signal, data set ready, active low<br>General GPIO2, input and output controlled by driver software |
| 16 | DCD1/<br>GPIO3 | IN /<br>(IN/OUT) | MODEM1 input signal, data carrier detect, active low<br>General GPIO3, input and output controlled by driver software |
| 15 | ACT# | OUT | USB configuration completed status output, active low, invalid when suspend |
| 14 | SUSPEND# | OUT | USB suspend state output, active low, output high level in normal working state, output low level after suspension |
| 3,4,13,19,<br>20,28,29,30,<br>31,32,33,39 | NC | / | No connection, must be suspended |

# 5. Functional description

## 5.1. Internal structure




## 5.2. Power and power consumption

CH9103 has 3 power supplies, built-in power regulator that generates 3.3V voltage. VDD5 is the input of power regulator, V3 is the output of power regulator, and USB transceiver and core power supply input, VIO is the I/O pin power supply.

CH9103 supports 5V or 3.3V supply voltage, the V3 pin should be externally connected to an external power decoupling capacitor of about 0.1uF. When using 5V power supply (more than 3.8V), VDD5 pin inputs external 5V power supply (for example, the USB bus power supply), the internal power regulator generates 3.3V on V3 pin which used for USB transceiver. When using 3.3V or lower operating voltage (less than 3.6V),

V3 pin should be connected to VDD5, and input external 3.3V power supply simultaneously. V3 still need to connect with an external power decoupling capacitor.

The VIO pin of CH9103 is used to provide I/O power supply to the two serial port pin I/O and RST, and supports 1.8V~5V supply voltage. VIO, MCU and other peripheral devices should use the same power supply. UD+, UD- and VBUS use V3 power supply, not VIO power supply.

CH9103 supports automatically USB device suspension to save power consumption. In the USB suspend state, if there is no external load on the I/O output pins, and the I/O input pins are suspended (internal pull-up) or high level state, then VIO power supply will not consume current. In addition, when V3 and VDD5 lose power supply and are at 0V voltage, the current consumption of VIO is the same as above, and VIO will not backflow current to VDD5 or V3.

VBUS pin should be connected to USB bus power supply, and when the missing of USB power is detected, CH9103 will turn off the USB and to sleep (suspend). The VBUS pin has a built-in pull-down resistor, which can be controlled by setting the OUT1 signal in the serial port MCR register using the software on the computer side(SERIAL_IOC_MCR_OUT1), turn on the pull-down resistor when OUT1 is invalid (default state), and turn off it when OUT1 is valid.

CH9103 provides VIO low-voltage protection mechanism when VBUS connects resistor in series which used to control VIO power through PMOS. During the period when the VBUS pull-down resistor is turned off, if the VIO voltage is detected to be below approximately 1.4V, then the CH9103 will automatically absorb a discharge current of approximately 300uA at the VBUS pin until it ends when the VIO voltage rises and the pull-down resistor is automatically turned on.

Several power supply connection schemes for reference here:

<table>
<tr><td rowspan="2">Power supply scheme</td><td rowspan="2">UART signals voltage<br>MCU operating voltage</td><td>VDD5 pin</td><td>V3 pin</td><td>VIO pin</td><td>MCU or peripheral power supply</td></tr>
<tr><td>Not less than V3 voltage</td><td>Rated around 3.3V</td><td colspan="2">Both use the same power supply, 1.8V～5V</td></tr>
<tr><td rowspan="4">All USB power supply</td><td>5V</td><td>USB powered 5V</td><td>Connect to capacitor only</td><td colspan="2">USB powered 5V</td></tr>
<tr><td>3.3V</td><td>USB powered 5V</td><td>Connect to capacitor</td><td colspan="2">V3 powered 3.3V, up to 10mA</td></tr>
<tr><td>3.3V</td><td colspan="4">USB powered 5V stepped down to 3.3V via external LDO power regulator, V3 connects to external capacitor</td></tr>
<tr><td>1.8V～4V</td><td>USB powered 5V</td><td>Connect to capacitor only</td><td colspan="2">USB powered, step-down via external LDO regulator</td></tr>
<tr><td>USB+ self-powered Dual power supply</td><td>1.8V～5V</td><td>USB powered 5V</td><td>Connect to capacitor only</td><td colspan="2">Self-powered 1.8V～5V (1.8V, 2.5V, 3.3V, 5V)</td></tr>
</table>

| | | | | |
|---|---|---|---|---|
| All self-powered | 4V～5V | Self-powered 4V～5V | Connect to capacitor only | Self-powered 4V～5V |
| | 1.8V～5V | Self-powered, rated 3.3V, connects to external capacitor | | Self-powered 1.8V～5V |

Recommended dual power supplies scheme, only VIO and MCU use the same power supply, low-current consumption, VIO current is only 2uA when USB suspend or sleep.

## 5.3. UART

In UART mode, the pins of CH9103 chip include: data transfer pins, MODEM contact signal pins and auxiliary pins.

Data transfer pins include: TXD and RXD. RXD is high when UART input is idle. TXD is high when UART output is idle.

MODEM contact signals include: CTS, DSR, DCD, DTR and RTS. All these MODEM contact signals are controlled and function defined by computer application.

Auxiliary pins include: SUSPEND# and ACT#, etc.

SUSPEND# is the output pin of chip suspended state. When the chip is in a normal operating state, SUSPEND# outputs high level, and when the chip is in suspended state, SUSPEND# outputs low level.

ACT# is output pin of the USB device configuration completed state, which can be used to notify the MCU, or as a driver LED connected to VIO in series with a current limiting resistor.

If installing VCP vendor driver, some pins can map to common GPIO function.

The UART of CH9103 supports CTS and RTS hardware automatic flow control, which can be enabled by software. If enabled, UART will continue to send the next data only when CTS input is valid (active low), otherwise the UART transmission will be stopped; when the receive buffer is empty, UART will automatically set RTS to be valid (active low), it will automatically invalidate RTS until the data in the receive buffer is nearly full, and RTS will be valid again when the buffer is empty. While using hardware automatic flow control, CTS pin of CH9103 should connect to RTS of the counterpart, and RTS of CH9103 should connect to CTS of the counterpart.

CH9103 has integrated separate transmit-receive buffer and supports simplex, half-duplex or full-duplex asynchronous serial communication. Serial data contains one low-level start bit, and 5, 6, 7 or 8 data bits and 1 or 2 high-level stop bits, supports odd/even/mark/space parity. CH9103 supports common communication baud rate: 50, 75, 100, 110, 134.5, 150, 300, 600, 900, 1200, 1800, 2400, 3600, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 56000, 57600, 76800, 115200, 128000, 153600, 230400, 256000, 307200, 460800, 1M, 1.5M, 2M, 3M, etc.

In applications with higher communication baud rate, it is recommended to enable hardware automatic flow control. Full-speed USB is only 12Mbps, considering the protocol overhead and other factors, in practical applications, the dual UARTs should be avoided in a continuous or full-duplex of 1Mbps and above high-speed communication status at the same time.

The allowable baud rate error of the CH9103 UART receive signal is not more than 2%, and the baud rate error of UART transmit signal is less than 1.5%.

In the Windows OS, CH9103 supports the CDC class drivers that come with the system, and can also install high speed VCP vendor driver, it can also emulate standard serial ports, so most serial port applications are fully compatible and usually do not require any modification.

CH9103 can be used to upgrade the original UART peripheral devices, or expand extra UART for computers via USB bus. Further interfaces such as RS232, RS485, RS422 can be provided through the addition of level conversion devices.

### 5.4. Clock, reset and others

CH9103 has a built-in USB pull-up resistor, and the UD+ and UD- pins should be directly connected to the USB bus.

CH9103 has a built-in power-on reset circuit, and also provides an external reset input pin with active low level. When the RST pin is at a low level, CH9103 will be reset; when the RST pin returns to a high level, CH9103 internal will continue to delay reset for about 15mS, and then enter the normal working state

CH9103 has a built-in low-voltage reset circuit, and monitors the voltage of the V3 pin and VIO pin at the same time. When the voltage of V3 is lower than VRV3 or the voltage of VIO is lower than VRVIO, the chip will be automatically hardware reset.

CH9103 has built-in clock generator, without external crystal and oscillation capacitor.

### 5.5. Parameter configuration

In larger batch applications, the CH9103's vendor identification code (VID), product identification code (PID) and product information can be customized.

In less batch applications, after installs VCP vendor driver, through configuration tool CH34xSerCfg.exe provided by chip manufacturer, users can be flexibly configure the vendor identification code (VID), product identification code (PID), maximum current value, BCD version number, vendor information and product information string and other descriptor, etc.

## 6. Parameters

### 6.1. Absolute maximum ratings

Critical state or exceeding maximum value may cause the chip to work abnormally or even be damaged.

| Name | Parameter Description | Min | Max | Unit |
|---|---|---|---|---|
| TA | Operating ambient temperature | -40 | 85 | ℃ |
| TS | Storage ambient temperature | -55 | 125 | ℃ |
| VDD5 | USB power supply voltage(VDD5 connects to power, GND to ground) | -0.5 | 6.0 | V |
| VIO | Serial port I/O power supply voltage(VIO connects to power, GND to ground) | -0.5 | 6.0 | V |
| VVBUS | VBUS voltage | -0.5 | 6.5 | V |
| VUSB | USB signal voltage | -0.5 | V3+0.5 | V |

| | | | | |
|---|---|---|---|---|
| VUART | Voltage on UART and other pins | -0.5 | VIO+0.5 | V |

## 6.2. Electrical characteristics

Test conditions: TA=25℃,VDD5=5V or VDD5=V3=3.3V, VIO=1.8V~5V, exclude USB pin

| Name | Parameter Description | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VDD5 | USB power supply voltage | V3 not connect to VDD5, V3 connects to capacitor | 4.0 | 5 | 5.5 | V |
| | | V3 connects to VDD5, VDD5=V3 | 3.0 | 3.3 | 3.6 | V |
| VIO | Supply voltage of the serial port and other I/O | | 1.7 | 5 | 5.5 | V |
| IVDD | Operating supply current of VDD5 or V3 | | / | 3 | 15 | mA |
| IVIO | VIO operating supply current (depends on I/O load) | | / | 0 | (10) | mA |
| ISLP | Operating supply current(USB suspend) | VDD5 power supply =5V | / | 0.09 | 0.16 | mA |
| | | VDD5=V3 power supply =3.3V | / | 0.085 | 0.15 | mA |
| | | VIO power supply, no I/O load/pull up | / | 0.002 | 0.05 | mA |
| ILDO | External load capacity of internal power regulator | | / | / | 10 | mA |
| VIL | Low level input voltage | VIO=5V | 0 | / | 1.5 | V |
| | | VIO=3.3V | 0 | / | 0.9 | V |
| | | VIO=1.8V | 0 | / | 0.5 | V |
| VIH | High level input voltage | VIO=5V | 2.5 | / | VIO | V |
| | | VIO=3.3V | 1.9 | / | VIO | V |
| | | VIO=1.8V | 1.3 | / | VIO | V |
| VIHVBS | High level voltage of VBUS | VIO=1.8～5V | 1.7 | / | 5.8 | V |
| VOL | Low level output voltage | VIO=5V, 15mA sunk current | / | 0.4 | 0.5 | V |
| | | VIO=3.3V, 8mA sunk current | / | 0.3 | 0.4 | V |
| | | VIO=1.8V, 3mA sunk current | / | 0.3 | 0.4 | V |
| VOH | High level output voltage Non-reset status | VIO=5V, 10mA output current | VIO-0.5 | VIO-0.4 | / | V |
| | | VIO=3.3V, 5mA output current | VIO-0.4 | VIO-0.3 | / | V |
| | | VIO=1.8V, 2mA output current | VIO-0.4 | VIO-0.3 | / | V |
| IPUP | Pull-up current of serial port and RST (pull-up to VIO voltage) | VIO=5V | 35 | 150 | 220 | uA |
| | | VIO=3.3V | 15 | 60 | 90 | uA |
| | | VIO=1.8V | 3 | 14 | 21 | uA |
| IPDN | Pull-down current of VBUS | VBUS>1.6V | 6 | 10 | 16 | uA |
| | | VBUS<1.3V | 50 | 140 | 200 | uA |

| | | | | | |
|---|---|---|---|---|---|
| VRV3 | Power-on reset / low voltage reset voltage threshold of V3 power | 2.5 | 2.7 | 2.9 | V |
| VRVIO | Low voltage reset voltage threshold of VIO power | 0.8 | 1.0 | 1.15 | V |
| VESD | HBM ESD withstand voltage on USB or I/O pins | 5 | 6 | / | KV |

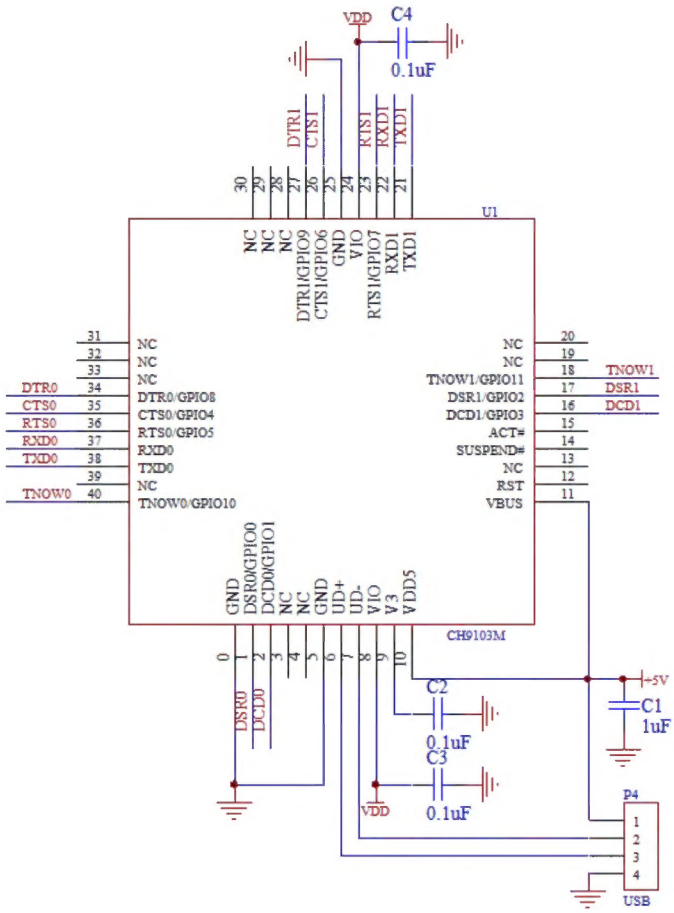
## 6.3. Timing parameters

Test conditions: TA=25℃,VDD5=5V or VDD5=V3=3.3V, VIO=1.8V～5V

| Name | Parameter Description | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FD | Error of internal clock (Equiproportional impact on baud rate) | TA=-15℃～60℃ | -1.0 | ±0.5 | +1.0 | % |
| | | TA=-40℃～85℃ | -1.5 | ±0.8 | +1.5 | % |
| TRSTD | Reset delay after power on or external reset input | | 9 | 15 | 25 | mS |
| TRI | Effective signal width of RST external reset input | | 100 | / | / | nS |
| TSUSP | Detect USB auto suspend time | | 3 | 5 | 9 | mS |
| TWAKE | Wake-up completion time after chip sleep | | 1.2 | 1.5 | 5 | uS |

# 7. Applications

## 7.1. USB to dual 9-line TTL UART




The figure above is the USB to TTL converter realized by CH9103. The only signal lines in the diagram that need to be connected are RXD, TXD, and the common ground. Other signal lines are selected as needed and can be suspended when not needed.

P4 is USB port, the USB bus includes a pair of 5V power lines and a pair of data signal lines. the +5V power line is red, the ground line is black, D+ signal line is green and the D- signal line is white. The USB bus can provide power supply current up to 500mA, the VBUS pin detects the USB power supply status here.

The capacitor C2 on V3 is 0.1uF which is used for CH9103 internal power node decoupling. C1, C3 and C4 are used for external power decoupling.

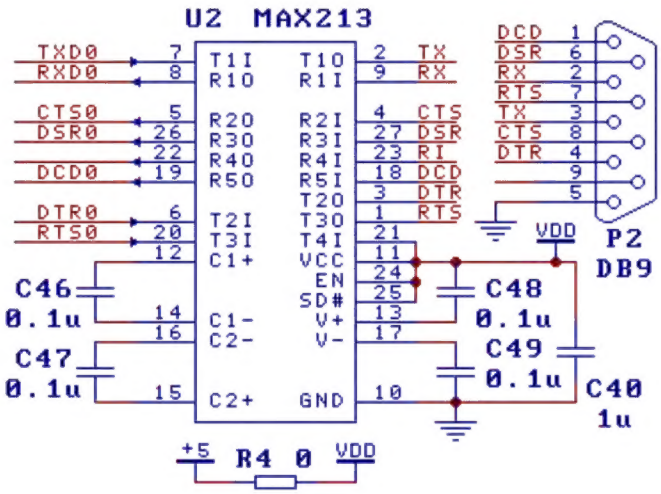
The capacitor C3 can be omitted if VIO is already shorted to V3 in the application. In VIO=V3=VDD5 all self-powered 3.3V case, capacitor C2 and C3 can be omitted.

Three power supply schemes: One is all USB power supply, CH9103 and USB products directly use the 5V power supply provided by the USB bus, that is, VDD5=VBUS=USB 5V power, VIO=VMCU=USB 5V or 1.8V~4V after step-down; The second is separate and independent power supply. The VIO of CH9103 and the MCU of the product use self-supplied standing power VDD, while CH9103 uses USB power, and its VDD5 is connected to the USB power VBUS, that is, VDD5 = BUS = USB 5V power, VIO = VMCU = VDD = self-supply 1.8V~5V; The third is all self-powered, only detecting but not using USB power, USB products provide power VDD through self-powered mode, mainly VDD5 = VIO = VMCU =VDD=self-supplied 5V or

VDD5 = V3 = VIO = VMCU = VDD = self-supplied 3.3 V two kinds.

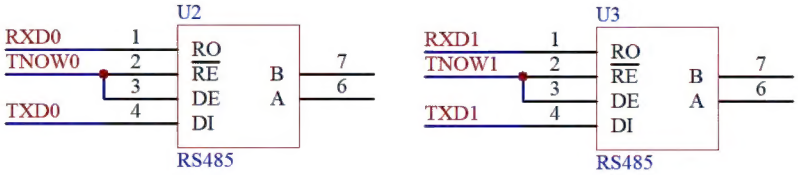
When designing the PCB, pay attention to: decoupling capacitor C1,C2,C3 and C4 should be as close as possible to the connected pins of CH9103; The D+ and D- signal lines are placed close to the parallel wiring, and surrounding the relevant components with ground lines or copper cladding can reduce signal interference from outside.

## 7.2. USB to dual 9-line RS232 UART




CH9103 provides common UART signals and MODEM signals, the figure shows that one of the TTL UART is converted to RS232 UART by external level conversion circuit U2. The other one is similar with this. Port P2 is DB9 connector, it has the same pins and functions as a normal 9-pin serial port of a computer, chip models similar to U2 include MAX213/ADM213/SP213/MAX211 etc.U2 in the image is uniformly powered by the USB bus through R4.

## 7.3. USB to dual RS485 UART




In the figure, TNOW is a switch pin to control the DE (active high transmit enable) and RE# (active low receive enable) pin of RS485 transceiver. The RS485 transceiver should use the same power supply as the VIO.